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Design and Simulation of a Novel Nine-Level Inverter for Solar Photovoltaic Systems

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***Abstract**: Some of the limitations of inverters can be solved by using a multilevel inverter topology. The number of level rises with the power quality and output voltage of the multilevel inverter also increases the level of harmonics. In this paper, seven and nine level modified multi-level inverter is introduced. The cascaded H-bridge multi-level inverters with different DC sources are discussed in detail with simulation results. In multilevel inverter, number of switches in cascaded H-bridge are increased when the number of output voltage levels increase. Numbers of ON state switches are large so that switching losses are also large in cascaded H-Bridge multilevel inverter. To reduce large quantity of switches a modified topology is used. Compared with cascade H-bridge multi-level inverter, the changed topology improves the quality. If the levels are raised, then fewer switches than the cascaded H-bridge inverter are needed in the changed topology. This reduces the initial costs and the length of the circuit, which also applies to industries. This paper explains the work on the modified topology. For the generation of appropriate switching pulses, both MLI topology pulse generators are used.*

***Key Word**: Solar; Photovoltaic; Multilevel Inverters; Simulation; Converters; IGBT; Switching.*

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I. Introduction

Power converters in electronics, mainly PWM DC as well as AC inverter, expanded their range of use in the industry, providing lower energy consumption, improved system performance, improved product quality, and good maintenance. Multilevel converters have been the more popular usage for traction, locomotives, or static converters on the trackside[4]. In many of the latest applications, VAR compensation, and stabilization power system converters[5], active filters[6], motor drivers of high voltage[3], transmission of dc high voltage[7], and most currently the variable motor induction drives[8] are among the most recent applications. Several multi-level conversion systems are based on motors drive of industrial medium-voltage[3,9], renewable energy devices of the utility interface type[10], the adjustable transmission AC system (FACTS)[11] and traction drive device[12].

Several multi-level inverter circuit topologies have been researched and utilized to solve the above problem effectively. The multilevel inverter's output voltage is composed of several levels which are synthesized from various direct current voltage sources. If the number of voltage stages raises, the output voltage quality improves, allowing the number of output filters to be reduced.

II. Basics and Background of Inverters

Multilevel technology based on medium-voltage-semiconductors is currently in developmentraces by conventional power inverter based on high-power semiconductor that are still in the early stages of development and are not yet mature. While conventional inverter is better for low power usage that does not meet the high power requirements given later, these should know the multi-level technology and the advantages it offers to recover the demerits of traditional inverters. For power applications, multi-level inverters are a reasonable alternative as these can achieve fairly high output.

Semiconductor technologies with medium power ratingsas compared to the traditional and well-known two-level converter, multilevel inverters provide significant advantages. The addition of devices to serial voltage capacity increases in other ways[11]. This solution allows inverters to meet high demands for power somehow. However, the output voltage efficiency is one of the greatest limitations. Therefore, with the classical device converter, only two levels of output can be produced. Such waveforms are actually composed of an enormous harmonic material, particularly low-range harmonics such as 3rd, 5th, 7th, etc. These harmonics have a significant impact on the equipment's output. Several low filters are frequently used to remove such harmonics and increase the efficiency at the output end. However, if the output is low, the filter size is still larger. Furthermore, the design of low pass filters is a well established fact that is a time-consuming task that is also

bulky in nature. There is a lot of research being done in this area, which focuses on reducing the size of filters in circuits[12,13]. In general, the following are the issues with traditional inverters:

a) When any switch is off the whole DC voltage is shown. This is higher than the individual devices' voltage rating.
b) Devices cannot share voltage automatically because of leak current differences - a parallel higher-value resistor may be utilized to resolve this (static sharing).
c) The most sincere, when switching systems do not share voltage because of differences in rpm. Special gate drive methods &/or snubber are needed (dynamic sharing).
d) 2-level output creates much large load voltage steps – motor insulation may be a concern.
e) For the given switches frequency, harmonic content 'distortion' is bigger than for the multi-level techniques

III. Modulation Techniques

For minimizing distortion, the low pulse numbers require the most efficientmodulation. Multi-level converters will significantly decrease the distortion, stagger the switching moment of the many switches and increase the apparent number of thetotalpulse of the converter under these conditions.

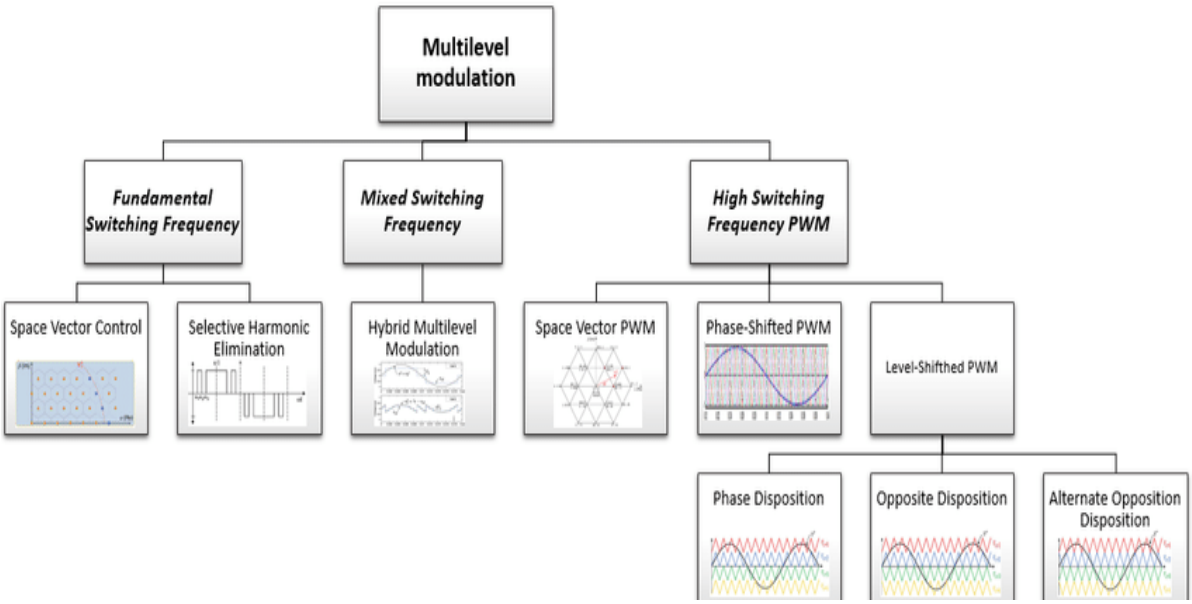

Figure 1 Details of PWM Techniques

The basic pulse width modulation methods are subdivided into conventional voltage sources and current-controlled techniques. The Digital Signore Processor (DSP) or Programmable Logic System (PLD) implementation is more readily available through voltage source methods. Still, current controls usually rely on event planning and are analog executions that may only be controlled consistently to some power level. The harmonic output is not considered as powerful as voltage source approaches in discrete current-controlled methods. The following is a sample PWM process.

The multi-level inverter carrier modulation schemes can usually be separated into two types:

1. phase -shifted
2. level-shifted

The phase -shifted cases have different types as:

1. In-phase deposition (IPD) where all waveforms of the carrier at the same phase.
2. Phase opposition disposition (POD), wherever the over null and below null waveforms are both phase and 180/ phase.
3. Alternate Phase Opposition Disposition (APOD).

IV. Results and Discussion

Table 1 System parameters

System parameters	Value
Reference frequency	50Hz
Carrier frequency	1200 Hz
Load resistance	1Ω
Load inducatnce	3mH
DC sources	E1=12V,E2=24V,E3=12V

Table 2 System parameters

Level of voltage	Modes	Load voltage(V)	ON mode switches
0	1	0	G1G2G3G4
E1	2	12	S1G2G3G4
E2	3	24	S3G4G1G2
E1+E2	4	36	S1S2S3G2
E1+E2+E3	5	48	S1S3G2G4
0	6	0	S1S2S3S4
-E1	7	-12	G1S2S3S4
-E2	8	-24	G1S2S3S4
-(E1+E2)	9	-36	G3G4G1S2
-(E1+E2+E3)	10	-48	G1S4G3S2

The topology functioning may be understood using its working states. Switching of pairs (Sj,Gj') {j = 1,2,3,4} shall be principal and complementary to the structure seen in Figure 2. There is a synthesization of ten working states by switching states of three independent switches S1, S2, S3 & S4. Fig.2 shows all working conditions. Two null states (1 and 6) and eight non-zero states are present. The load is fed at nine stages for all these operating states. Four switches concurrently load to a certain voltage level that is observable. To synthesize, for instance, Vo(t) = 4VDC, S1, S2, S2, S3, S4 switches lead during the remaining block of the switches. Also, for all positive & zero voltage levels (states 1 to 5), it should be stated here that the switch S2' is always conducive whereas the Switch S2 is always conducive for all levels of negative voltage (states 6 to 10). Thus, at a fundamental frequency, all switches can be operated to achieve all nine speeds. This is critical as the high voltage stress of 4VDC is addressed later on the S2 & the G2 switches.

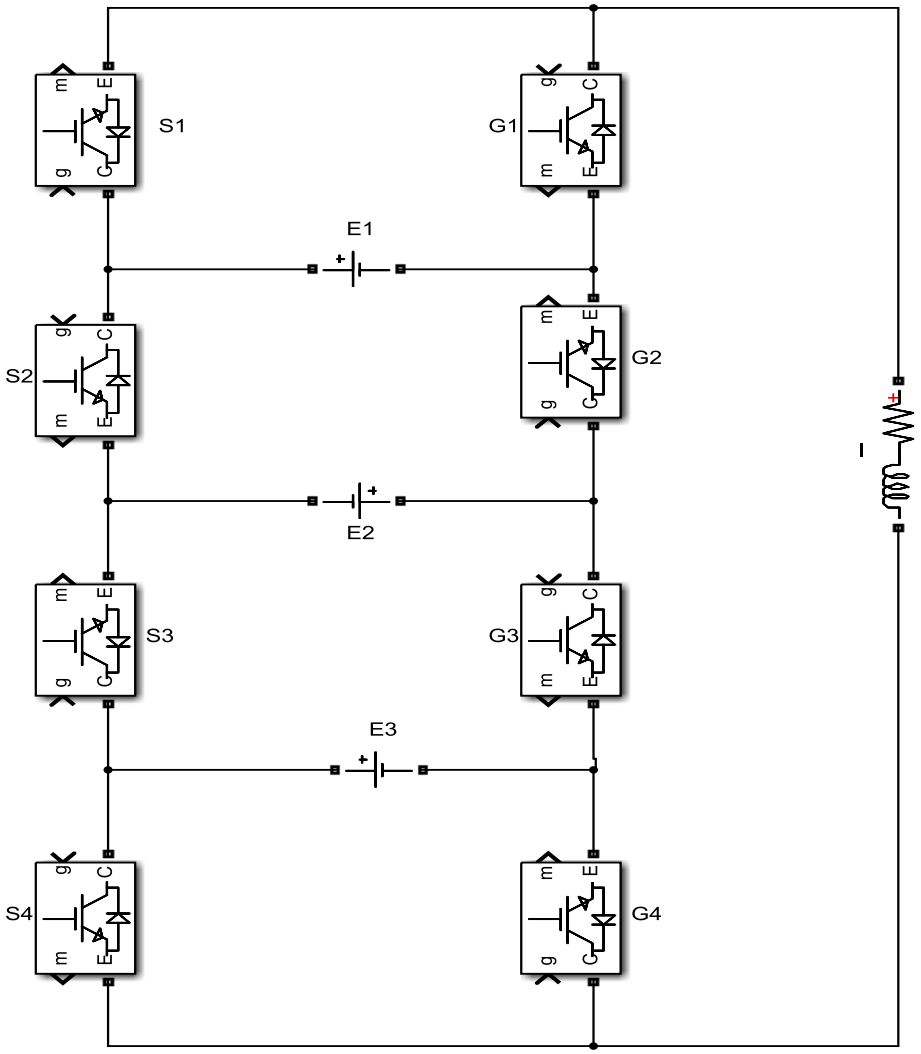

Figure 2 Switches and their Configuration

A switching process develops in this section to modulate the topology with the modulation of the multicarrier sine PWM. The system is built the switch of low current voltage stress (i.e. S1 & G1' switches) change by mover frequency though the switches of greatest current-voltage stress (i.e. S2 and G2' switches) switch by the basic frequency. The G4 & S4 switches work in an intermediary level frequency that is high compared to the general frequency, however significantly low comparison the carrier. They compared with the relation of every carrier indicates '1' when it is larger than the carrier & otherwise '0' The obtained 3 output waveforms (one per 3 Signals carriers) are applied to achieve the signal that has been 'aggregated' 'S(t)' signal added. The aggregated signal is seen in the waveforms.

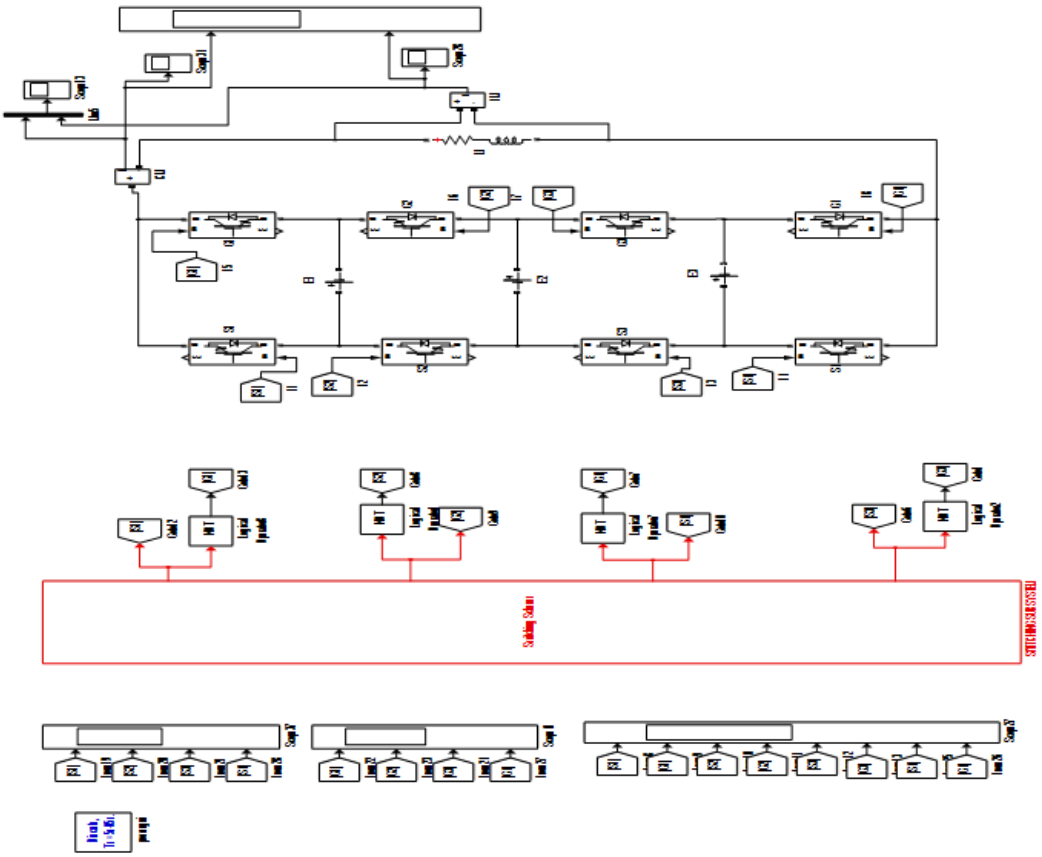

Figure 3 Canvas of MATLAB Simulation

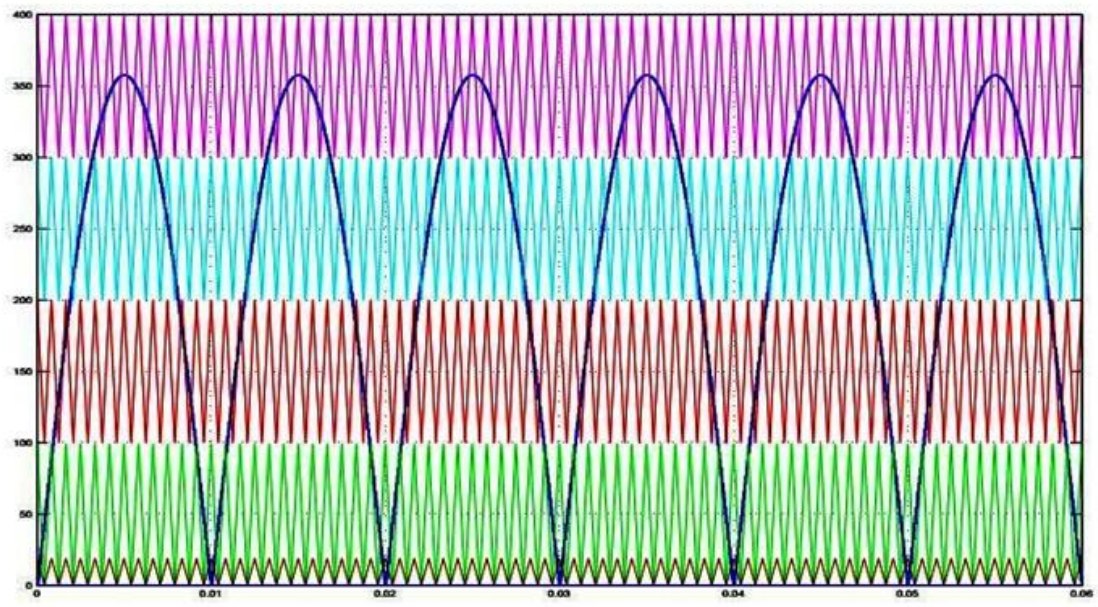

Figure 4 Signal Comparision

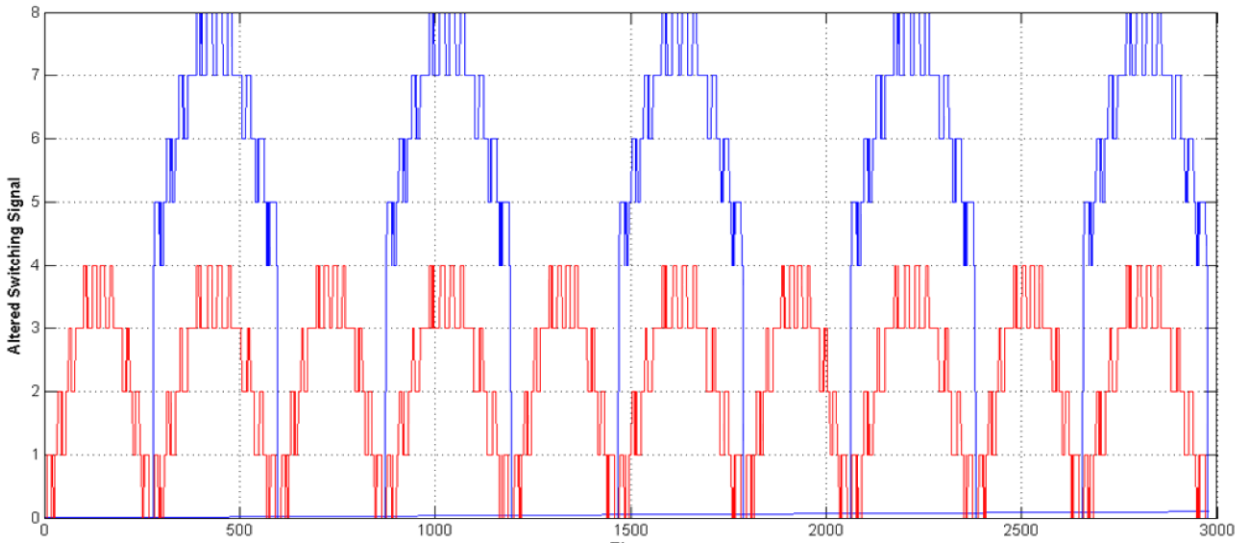

Figure 5 Altered Signal Aggregated

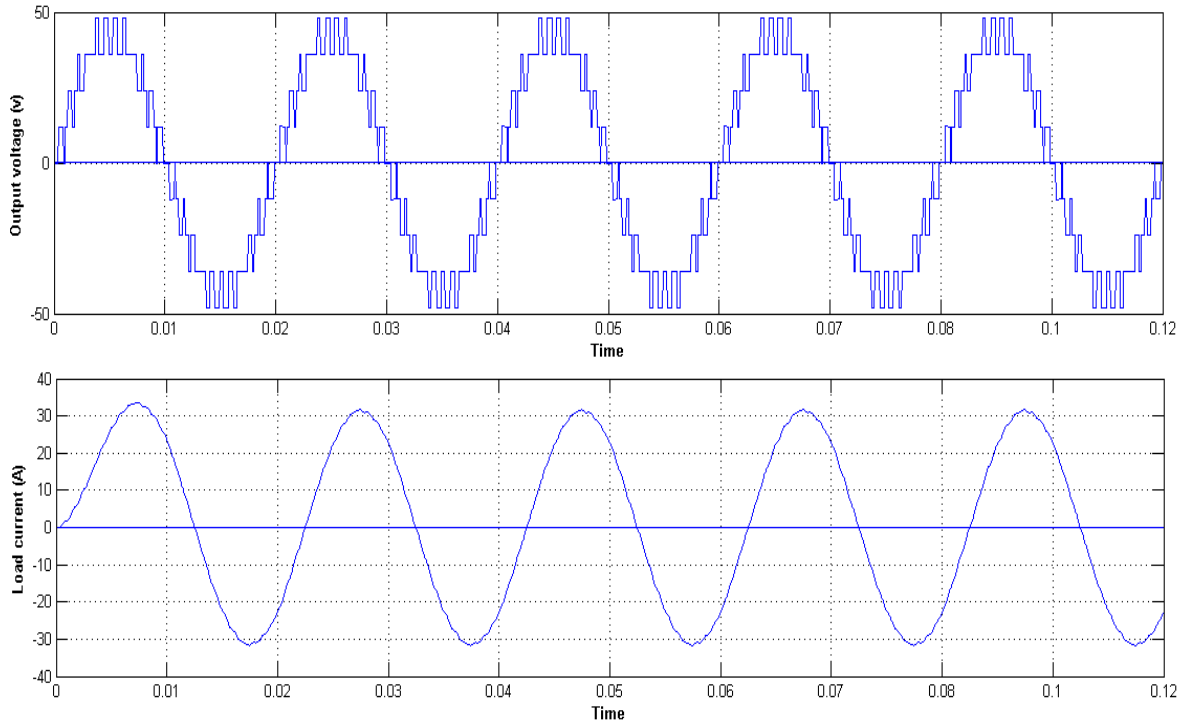

Figure 6 Simulation Results for Hybrid 9-level Inverter OutputVoltage and its Load Current

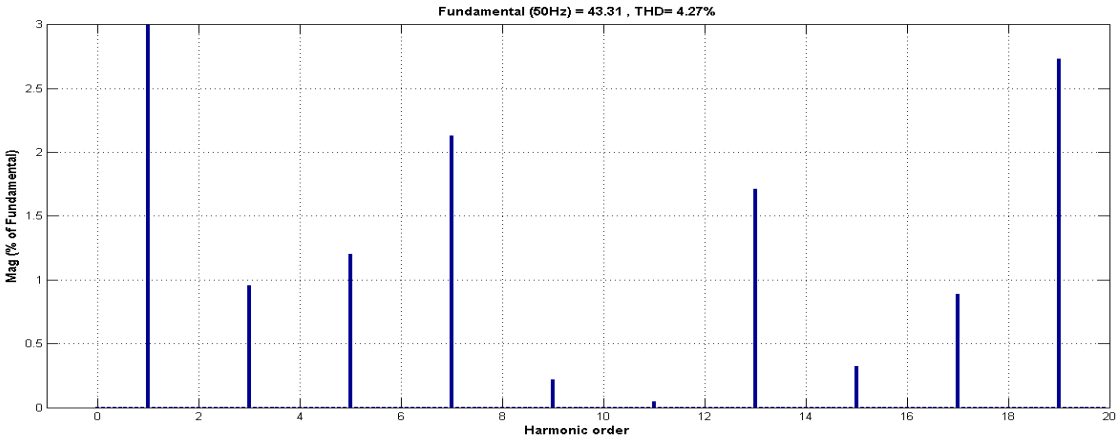

Figure 7 Harmonic profile of hybrid 9-Level Inverter (THD for output voltage)

V. Conclusion

The topologies of multilevel inverter circuits (7-level & 9-level) and their analysis is briefly discussed in this paper. Each MLI has its combination of benefits and drawbacks, and one topology would be more suitable than the other for any specific use. Topologies are often selected based on previous experiences, even though that topology is not the right fit for the application. Other technological drawbacks may be outweighed by the benefits of the body of study and favorably in the engineering communities. The abandonment of low order switching frequency terms in multilevel converters will result in an efficient increase in overall switch frequency.

Today, multilevel inverter-based technologies are being researched and developed worldwide research.

This paper focuses on the basic principles of various multilevel converters, modulation technology & harmonic studies. The first aspect is the failure safety analysis used for induction motors for cascaded inverter multi-level drive. Because of an extreme amount of semi-conductor and passive component systems, how a failure management system can be designed to improve travel – although it remains an important problem in different fault scenarios. The defective module should be removed in automotive applications when the converter works. A further transition is then essential for the module connections at the terminal points. Experimental experiments have shown that the voltage is spread equitably among the other modules when this error occurs, such that it corresponds to the DC connection voltage. The reliability of the device is thus guaranteed under module defect conditions.

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